**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

Claim 1 (Canceled)

Claim 2 (Currently Amended): The semiconductor device according to claim 13 [[1]], wherein ~~the semiconductor chips include first and second semiconductor chips, the second semiconductor chip is mounted on the first semiconductor chip as~~ the back side of the second semiconductor chip faces the front side of the first semiconductor chip, and a passivation film is formed on the front side of the second semiconductor chip.

Claim 3 (Canceled)

Claim 4 (Withdrawn – Currently Amended): The semiconductor device according to claim 13 [[3]], wherein the first post electrode formed on the second conductive pattern is formed near almost a center part of the second conductive pattern ~~wiring~~.

Claim 5 (Withdrawn – Currently Amended): The semiconductor device according to claim 13 [[1]], wherein ~~the semiconductor chips include first and second semiconductor~~

~~chips, the second semiconductor chip is mounted on the first semiconductor chip as~~ the back side of the second semiconductor chip faces the front side of the first semiconductor chip, and wherein the semiconductor device further includes

~~a first post electrode formed on the first conductive pattern for electrically connecting between the first wiring and the external terminal, and~~

[[a]] second post electrodes ~~electrode~~ formed on the front side near a [[the]] periphery of the first semiconductor chip simultaneously with the first post electrodes ~~electrode~~, the second post electrodes are recognition posts that identify ~~electrode for recognizing~~ the periphery of the first semiconductor chip.

Claims 6-7 (Canceled)

Claim 8 (Withdrawn – Currently Amended): The semiconductor device according to claim 20 [[7]], wherein the first conductive pattern is provided with an opening part, and one of the projecting electrodes ~~electrode~~ is placed on the opening part of the first conductive pattern.

Claim 9 (Withdrawn – Currently Amended): The semiconductor device according to claim 20 [[7]], wherein the first conductive pattern is provided with a recess, and one of the projecting electrodes ~~electrode~~ is placed on the recess of the first conductive pattern.

Claim 10 (Withdrawn – Currently Amended): The semiconductor device according to claim 20 [[7]], wherein the projecting electrodes are ~~electrode is~~ connected to the first conductive pattern through an adhesive material.

Claim 11 (Withdrawn – Currently Amended): The semiconductor device according to claim 15 [[1]], wherein ~~the semiconductor devices includes first and second semiconductor chips, and~~ the front side of the second semiconductor chip is connected to the front side of the first semiconductor chip through an adhesive material.

Claim 12 (Withdrawn – Currently Amended): The semiconductor device according to claim 13 [[1]], ~~wherein the semiconductor chips includes first to~~ further comprising a third semiconductor chip having a front side, a back side, and third pad electrodes on the front side thereon,

wherein ~~chips, the second semiconductor chip is mounted on the first semiconductor chip as~~ the front side of the second semiconductor chip faces the front side of the first semiconductor chip, and ~~the third semiconductor chip is mounted on the second semiconductor chip as~~ the back side of the third semiconductor chip faces the back side of the second semiconductor chip.

Claim 13 (New): A semiconductor device comprising:

a first semiconductor chip having a front side, a back side, and first pad

electrodes formed on the front side and electrically connected to an integrated circuit formed on the front side;

a first conductive pattern which is composed of a first conductive layer and which is electrically connected to one of the first pad electrodes;

a second conductive pattern which is composed of the first conductive layer and which is electrically connected to a second one of the first pad electrodes and another of the first pad electrodes adjacent to the second one of the first pad electrodes;

first post electrodes which are formed on the first conductive pattern and the second conductive pattern;

a second semiconductor chip having a front side, a back side, and second pad electrodes formed on the front side thereof, the second semiconductor chip being mounted on the front side of the first semiconductor chip;

a third conductive pattern which is composed of a second conductive layer and which is electrically connected to the first post electrodes;

an encapsulating resin which encapsulates the front surfaces of the first and second semiconductor chips; and

external terminals which are formed over the third conductive pattern and are electrically connected to the third conductive pattern.

Claim 14 (New): The semiconductor device according to claim 13, further comprising:

second post electrodes which are formed on the third conductive pattern and

wherein the external terminals are formed on the second post electrodes.

Claim 15 (New): A semiconductor device comprising:

a first semiconductor chip having a front side, a back side, and first pad electrodes formed on the front side and electrically connected to an integrated circuit formed on the front side;

a first conductive pattern which is composed of a first conductive layer and which is electrically connected to one of the first pad electrodes;

a second conductive pattern which is composed of the first conductive layer and which is electrically connected to a second one of the first pad electrodes and another of the first pad electrodes adjacent to the second one of the first pad electrodes;

first post electrodes which are formed on the first conductive pattern and the second conductive pattern;

a second semiconductor chip having a front side, a back side, and second pad electrodes formed on the front side thereof, the second semiconductor chip being mounted on the front side of the first semiconductor chip;

an encapsulating resin which encapsulates the front surfaces of the first and second semiconductor chips; and

external terminals which are formed over the encapsulating resin and which are electrically connected to the second conductive pattern and at least one of the second pad electrodes.

Claim 16 (New): The semiconductor device according to claim 15, wherein the back side of the second semiconductor chip faces the front side of the first semiconductor chip, and a passivation film is formed on the front side of the second semiconductor chip.

Claim 17 (New): The semiconductor device according to claim 16, further comprising a third conductive pattern which is composed of a second conductive layer and which is electrically connected to the first post electrodes.

Claim 18 (New): The semiconductor device according to claim 17, further comprising:

second post electrodes which are formed on the third conductive pattern and wherein the external terminals are formed on the second post electrodes.

Claim 19 (New): The semiconductor device according to claim 15, wherein the front side of the second semiconductor chip faces the front side of the first semiconductor chip.

Claim 20 (New): The semiconductor device according to claim 19, wherein the second semiconductor chip includes projecting electrodes on the front side thereof electrically connected to the first and second conductive patterns.